

Introduction

Traditionally, the design of large analog switching matrices has been based upon the use of electromechanical switches. As such, many moving parts were used in the construction of these switch matrices. With advances in electronics, electro-mechanical switches can now be replaced by equivalent semiconductor switches which offer more economical solutions as well as improved reliability. The Mitel family of analog crosspoint switch devices can be configured easily into various sizes of switch matrices due to the wide variety of switch array configurations and their excellent electrical performance.

The purpose of this application note is to show how a 3-stage non-blocking switch matrix can be implemented using the minimum number of Mitel switch arrays. The theory of optimizing the 3-stage

switch matrix will be discussed briefly and examples will be presented. The MT8816 8x16 crosspoint switch is used as the primary example because its large size will reduce the total number of devices for a particular switch matrix design. However, the exercise can be repeated easily with other Mitel switch arrays.

The most common method employed in analog switch matrix design is space division switching whereby signals are physically switched from one signal line to another. Unlike time division switching used in digital matrices, there is little delay added to the signal due to the switching mechanism. The actual delay is determined by the propagation time through the semiconductor switch and the local circuit. This, coupled with low values of on-resistance, allows matrices of different configurations to be built with little signal degradation.

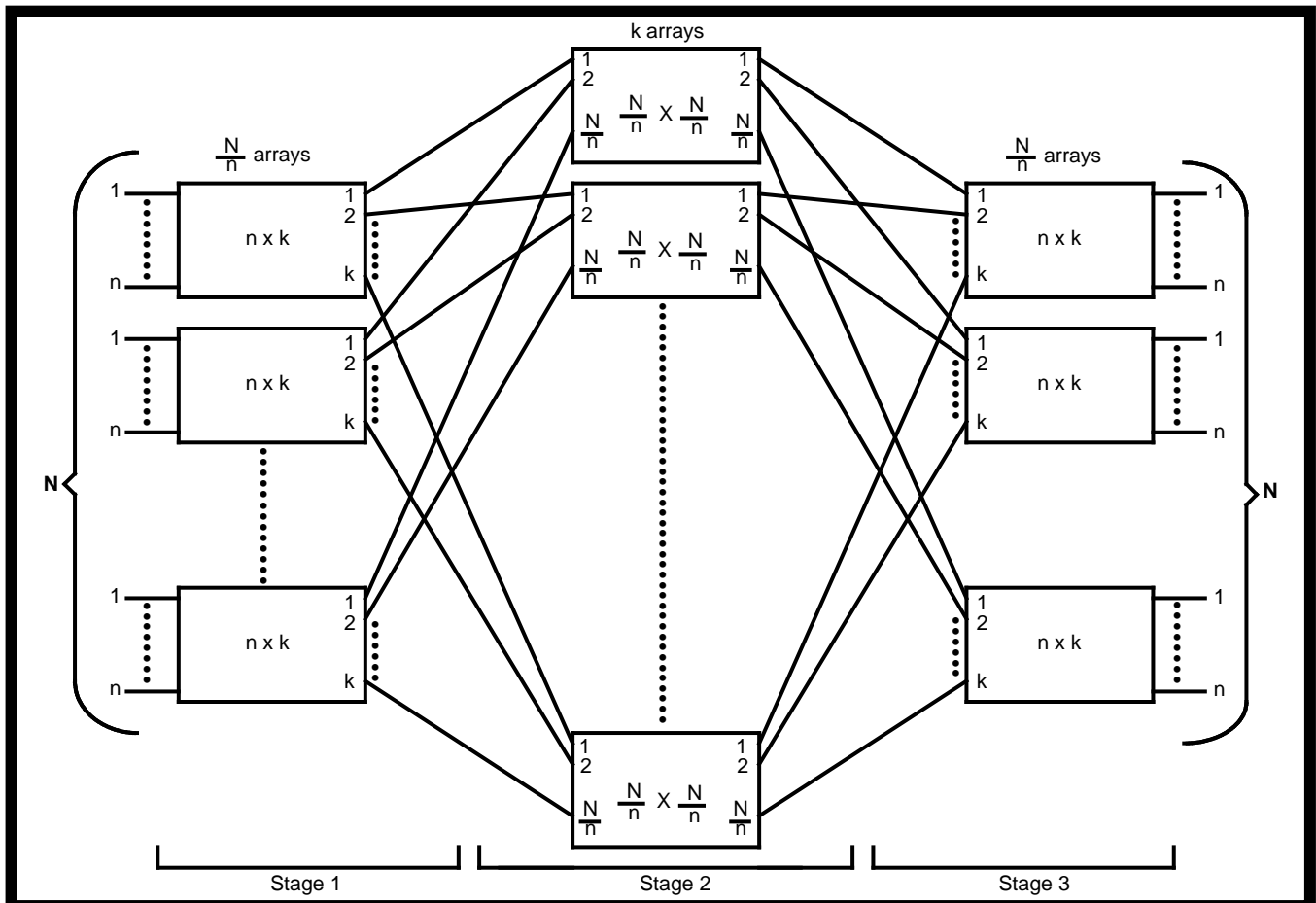


Figure 1 - Generalized 3-Stage Non-Blocking Switch Matrix for $N \times N$ Lines

Single State Solution

The simplest switching structure is a single stage non-blocking matrix consisting of an MxN rectangular array of crosspoints. This switch matrix can always make a connection from one of its M inputs/outputs to one of its N inputs/outputs regardless of any connections already established, e.g., MT8816 can connect any one of 8 Xi inputs/outputs to any one of 16 Yi inputs/outputs. Altogether there are 128 (8x16) crosspoint switches within the matrix. Normally for designing a system with a small matrix size, the number of analog switch arrays can be determined directly by their sizes.

Example # 1: Construct a 32x32 switch matrix using MT8816. The number of MT8816s in the vertical (Y) direction is given by 32÷16=2. The number of MT8816s in the horizontal (X) direction is given by 32÷8=4. Therefore, 8 (4x2) MT8816s will be required.

Multi-stage Solution

However, when the number of lines gets very large, the number of switch arrays can increase substantially. A 128x128 switch matrix will require 128 MT8816s for a NxN single stage matrix (where N denotes the line size of the switch matrix) and a 512x512 switch matrix will require 512 MT8816s. The number of crosspoints can be reduced using a multi-stage switch matrix. Of particular interest is the 3-stage non-blocking switch matrix which will provide significant savings in the number of crosspoints at the expense of increased signal attenuation (RON resistance being three times more than the single stage switch), and control software complexity. The former issue can be resolved by adding signal amplification in between the 3-state matrix, and at the same time, careful planning of the software can reduce its complexity.

Fig. 1 illustrates the general layout of a 3-stage NxN switch matrix. The first and third stages of the matrix are identical and each consists of (N÷n) switch arrays of size (nxk). The middle stage contains k switch arrays of size (N÷n)x(N÷n). It can be shown that for non-blocking matrices, the value k must be equal to (2n-1). The total number of crosspoints will be given by:

$$\begin{aligned}
 C_n &= 2(N\div n) nk + k(N\div n)^2 \\
 &= 2(N\div n) n (2n-1) + (2n-1) (N\div n)^2 \\
 &= (2n-1) [2N + (N\div n)^2]
 \end{aligned}$$

...Eq. (1)

To obtain the optimal value of n, differentiate Cn w.r.t. n and set the equation to 0:

$$\begin{aligned}
 \frac{dC_n}{dn} &= 2(2N+(N\div n)^2)-2(2n-1)(N\div n)^3=0 \\
 2n^3 - nN + N &= 0
 \end{aligned}$$

...Eq.(2)

As N gets very large, Eq. (2) can be approximated by:

$$\begin{aligned}
 2n^3 - nN &= 0 \\
 n_{(op)} &= \sqrt{\left(\frac{N}{2}\right)}
 \end{aligned}$$

...Eq.(3)

where n_(op) denotes the optimum value of n.

The optimum value of Cn, Cn_(op) can be found by substituting Eq. (3) into Eq. (1):

$$C_{n_{(op)}} = 4N \sqrt{2N - 1}$$

...Eq. (4)

where Cn_(op) denotes the minimum number of crosspoints.

Table 1 compares the number of crosspoints in a single-stage matrix versus a three-stage matrix for various line sizes.

Number of Lines (N)	Single Stage (N x N)	Three-Stage Cn _(op)
32	1,024	896
64	4,096	2,640
128	16,384	7,680
256	65,536	22,147
512	261,632	63,488
1024	1.0E06	181,268
2048	4.2E06	516,096

Table 1. Single Stage vs. Three-Stage Solution

Example #2: Construct a 3-stage 128°128 switch matrix.

- size of array (nxk) in stage 1 and stage 3 is=

$$\begin{aligned}
 n_{(op)} &= \sqrt{128\div 2} = 8 \\
 k &= 2n-1 = 2 \times 8 - 1 = 15
 \end{aligned}$$
- number of MT8816s in stage 1 and stage 3=

$$2 \times N \div n_{(op)} = 2 \times (128 \div 8) = 32$$
- size of array in stage 2 (N÷n)x(N÷n) is: 16x16. Each array requires 2 x MT8816s. The total number of state 2 arrays is: 2xk = 2x15 = 30.
- the total number of MT8816s is: 30 + 32 = 62.

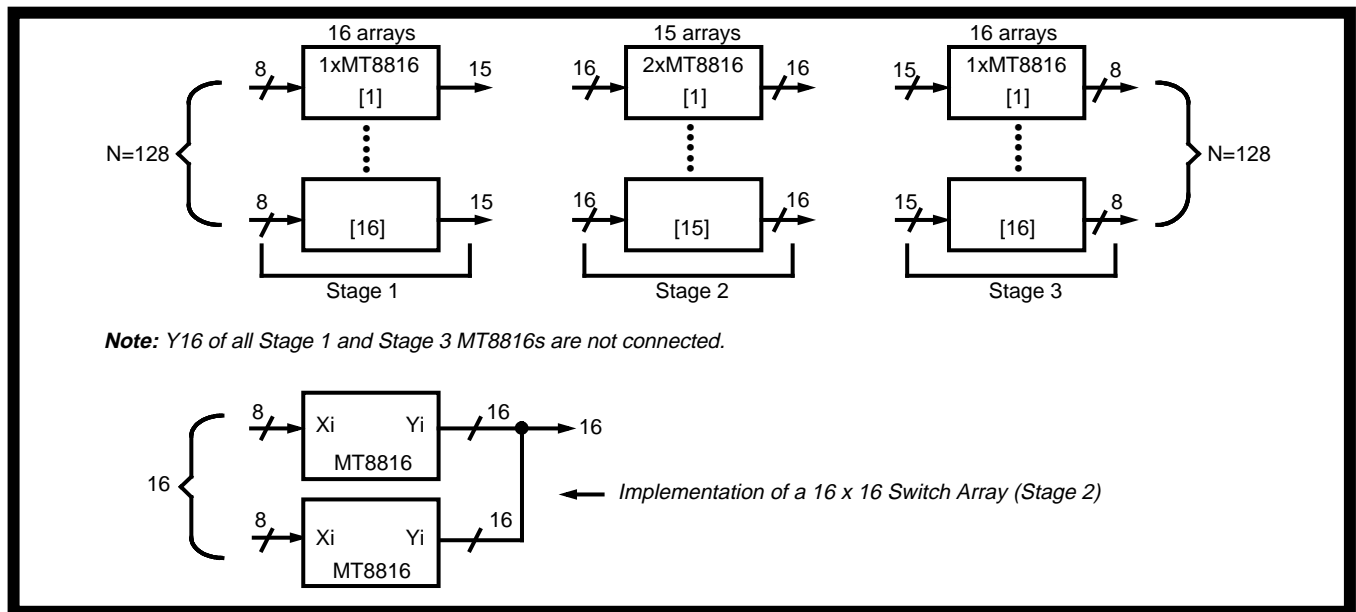


Figure 2 -A 128 x 128 Non-Blocking 3-Stage Switching Matrix

- The savings in MT8816s over the single stage solution is: $128 - 62 = 66$
- comparison of number of crosspoints:
 - single stage: $C_n(N \times N) = 128 \times 128 = 16,384$
 - 3-stage: $C_n = 66 \times 16 \times 8 = 8,448$
 - optimal 3-stage: $C_{n(op)} = 4 \times 128 \times [\sqrt{(256)} - 1] = 7,680$
- number of MT8816s in stage 1 and stage 3: $2 \times (N \div n) \times 4 = 2 \times (256 \div 16) \times 4 = 128$
- Size of array in the second stage is: $(N \div n) \times (N \div n) = 16 \times 16$. Each stage 2 array requires $(16 \div 16) \times (16 \div 8) = 2 \times$ MT8816s. The total number of MT8816s for stage 2 is: $2 \times k = 2 \times 31 = 62$
- Fig. 2 illustrates the structure of a 3-stage 128 x 128 switch matrix.
- the total number of MT8816s = $128 + 62 = 190$.
- Example #3: Construct a 3-stage 256 x 256 switch matrix using MT8816s.
- the savings in MT8816s over the single stage solution is: $512 - 190 = 332$.
- size of array (n x k) in stage 1 and stage 3 is: notice that $n_{(op)} = \sqrt{128 \div 2}$ is not an integral number, a better line size in this case is given by: $n = \sqrt{256} = 16$, $k = 2n - 1 = 2 \times 16 - 1 = 31$. Each stage 1 array requires: $(32 \div 16) \times (16 \div 8) = 4 \times$ MT8816s
- Comparison of number of crosspoints:
 - single stage: $C_n(N \times N) = 256 \times 256 = 65,536$
 - 3-stage: $C_n = 190 \times 16 \times 8 = 24,320$
 - optimal 3-stage: $C_{n(op)} = 4 \times 256 \times [\sqrt{(512)} - 1] = 22,147$

Line Size (N x N)	MT8816 (Single Stage)	MT8816s (3-Stage Matrix)			
		Stage 1 n x k	Stage 2 (N/n) x (N/n)	Stage 3 k x n	Total # of MT8816s
16 x 6	2	---	---	---	---
32 x 32	8	---	---	---	---
64 x 64	32	8(8 x 15)	8(8 x 8)	8(15 x 8)	24
128 x 128	128	16(8 x 15)	30(16 x 16)	16(15 x 8)	62
256 x 256	512	64(16 x 31)	62(16 x 16)	64(31 x 16)	190
512 x 512	2048	128(16 x 31)	248(32 x 32)	128(31 x 16)	504
1024 x 1024	8192	512(32 x 63)	504(32 x 32)	512(63 x 32)	1524
2048 x 2048	32768	1024(32 x 63)	2016(64 x 64)	1024(63 x 32)	4064

Table 2. Optimum Usage of MT8816 for Various Line Sizes up to 2048

Note: the individual array sizes are shown inside the brackets for a number of 3-stage matrices.

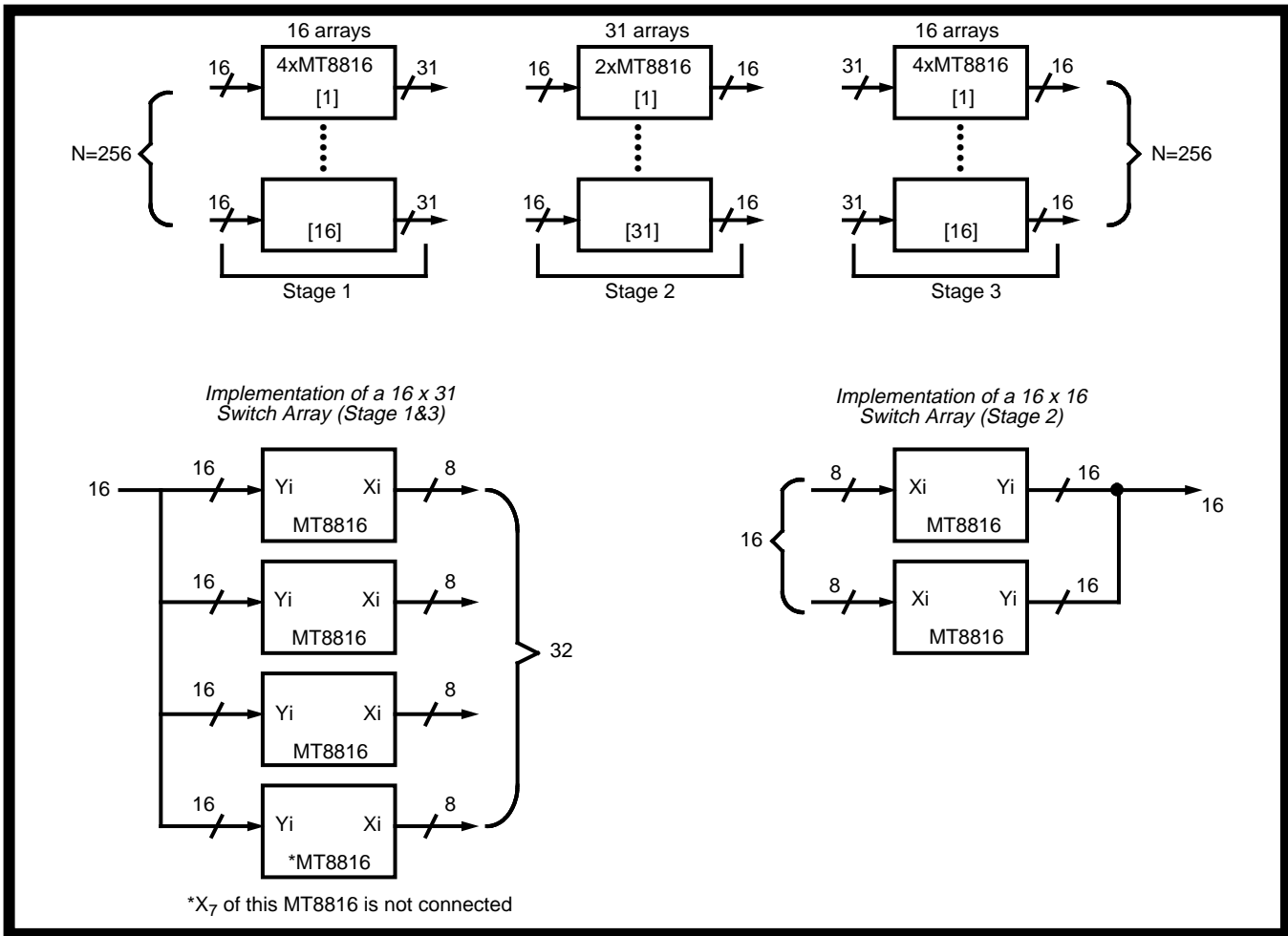


Figure 3 - A 256 x 256 Non-Blocking 3-Stage Switching Matrix

Fig. 3 illustrates the structure of a 3-stage 256° 256 switch array.

Table 2 summarizes the optimum usage of MT8816s for various line sizes up to 2,048.

Conclusion

As observed, even with the use of the 3-stage matrix, the number of switch arrays can be very large and makes the design uneconomical. The solution is to either to adopt higher stage switch matrix design (of more than three stages) or to introduce partial blocking without increasing the number of switch arrays.

References

Charles Clos, "A Study of Non-Blocking Switching Networks", Bell System Technical Journal, March 1953, pp. 406-424.

John Bellamy, Digital Telephony, pp. 220-242, pub. by John Wiley & Sons, 1982, ISBN 0-471-08089-6.